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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/975,296	10/12/2001	Xia Sheng	10016850-1	1287

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EXAMINER	
LEURIG, SHARLENE L	

ART UNIT	PAPER NUMBER
2879	

DATE MAILED: 02/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/975,296	Applicant(s) SHENG ET AL.	
	Examiner Sharlene Leurig	Art Unit 2879	AW

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 February 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2,3*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

2. Claims 1-6, 8, 11-23, 25 and 31-37 are rejected under 35 U.S.C. 102(a) as being anticipated by Iwasaki et al. (EP 1 117 118 A1) (of record).

Regarding claims 1 and 18, Iwasaki discloses an electron emitter device comprising an electron supply structure (Figure 22, elements 10, 11 and 12), at least one protrusion (21b) formed on a top surface of the electron supply structure, an insulator (13a) formed above the electron supply structure and the protrusion, and a top conductive layer (15a) formed on the insulator.

Regarding claims 2 and 19, Iwasaki discloses forming a conductive substrate made of a glass layer (10) having a metal layer formed thereon (11).

Regarding claims 3 and 20, the electron supply layer (12) is formed above the conductive substrate (10 and 11).

Regarding claims 4 and 21, the electron supply layer may be formed of a doped semiconductor (page 6, column 10, lines 14-16) or an undoped semiconductor (lines 7-8).

Regarding claims 5 and 22, the semiconductor, whether doped or undoped, can be formed of a polysilicon (column 10, lines 8-15).

Regarding claims 6 and 23, the areas of the silicon layer receiving the dopants can be interpreted as being "selectively doped" (column 10, lines 14-16).

Regarding claim 8, the insulator (13 and 13a) is substantially conformal to the electron supply structure including the protrusion.

Regarding claims 11 and 31, the insulator can be made of a diamond-like carbon, nitrides, carbides or oxynitrides of silicon, aluminum, titanium, tantalum, tungsten, hafnium, zirconium, vanadium, niobium, molybdenum, chromium, yttrium, scandium, nickel, cobalt, beryllium and magnesium (column 10, line 28 to column 11, line 22).

Regarding claims 12 and 32, the conductive substrate is formed of a metal coating (11) on glass (10) (column 9, lines 23-26).

Regarding claims 13 and 33, the metal coating on the conductive substrate can be made of aluminum, tungsten, titanium, copper, chromium or other metals (column 9, lines 24-26).

Regarding claims 14 and 34, the metal coating of the conductive substrate is patterned (Figure 33, element 11).

Regarding claims 15, 16, 35 and 36, the top conductive layer (Figure 22, element 15) is formed from a metal such as aluminum, tungsten, titanium, molybdenum, copper, gold, silver, tantalum, platinum, iridium, palladium, rhodium, chromium, scandium, yttrium, vanadium, zirconium, niobium, molybdenum, silver, osmium (column 11, lines 26-32).

Regarding claims 17 and 37, the top conductive layer (15) is patterned.

Regarding claim 25, the polysilicon can be formed by CVD or PVD (column 11, lines 39-50).

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-5, 8, 11-22, 25-27 and 31-37 are rejected under 35 U.S.C. 102(b) as being anticipated by Yoshikawa et al. (EP 0 878 819 A2) (of record).

Regarding claims 1 and 18, Yoshikawa discloses an electron emitter device comprising an electron supply structure (Figure 4, elements 10, 11 and 12), at least one protrusion (12) formed on a top surface of the electron supply structure, an insulator (13) formed above the electron supply structure and the protrusion, and a top conductive layer (15) formed on the insulator.

Regarding claims 2 and 19, a conductive substrate is formed of a glass or ceramic layer (10) having a metal layer formed thereon (11) (page 5, lines 50-51; page 7, lines 19-20).

Regarding claims 3 and 20, the electron supply layer (12) is formed above the conductive substrate (10 and 11).

Regarding claims 4 and 21, the electron supply layer may be formed of an undoped semiconductor (page 4, lines 11-14).

Regarding claims 5 and 22, the undoped semiconductor can be formed of a polysilicon (column 4, line 11).

Regarding claim 8, the insulator (13) is substantially conformal to the electron supply structure, including the protrusion.

Regarding claims 11 and 31, the insulator can be made of nitrides, carbides or oxynitrides of silicon, titanium, tantalum, tungsten, hafnium, zirconium, vanadium, niobium, molybdenum, chromium, yttrium, scandium, nickel, cobalt, beryllium and magnesium (Tables, pages 4 and 5).

Regarding claims 12 and 32, the conductive substrate is formed of a metal coating (11) on glass or ceramic (10) (page 5, lines 50-51; page 7, lines 19-20).

Regarding claims 13 and 33, the metal coating on the conductive substrate can be made of aluminum, tungsten or other metals (page 7, lines 19-20).

Regarding claims 14 and 34, the metal coating of the conductive substrate is patterned (Figure 9, element 11).

Regarding claims 15, 16, 35 and 36, the top conductive layer (Figure 4, element 15) is formed from a metal such as aluminum, tungsten, titanium, molybdenum, copper, gold, silver, tantalum, platinum, iridium, palladium, rhodium, chromium, scandium, yttrium, vanadium, zirconium, niobium, molybdenum, silver, osmium (page 5, lines 47-50).

Regarding claims 17 and 37, the top conductive layer (Figure 9, element 15) is patterned.

Regarding claim 25, the polysilicon can be formed by CVD or a PVD such as sputtering (page 3, lines 43-45).

Regarding claims 26 and 27, the insulator can be formed by oxidizing the polysilicon and the protrusion by thermal oxidation or plasma oxidation (page 3, lines 31-32 and 55-58).

5. Claims 1-3, 8-20 and 28-37 are rejected under 35 U.S.C. 102(b) as being anticipated by Kaneko et al. (EP 0 367 195 A2) (of record).

Regarding claims 1 and 18, Kaneko discloses an electron emitter device comprising an electron supply structure (Figure 11, element 1), at least one protrusion (1a) formed on a top surface of the electron supply structure, an insulator (21) formed above the electron supply structure and the protrusion, and a top conductive layer (33) formed on the insulator.

Regarding claims 2 and 19, the electron supply structure comprises a conductive substrate (1) (column 18, line 11).

Regarding claims 3 and 20, the electron supply layer (1a) is formed above the conductive substrate (1).

Regarding claim 8, the insulator (Figure 6a, element 2; Figure 11, elements 21 and 22) are conformal to the electron supply structure, including the protrusion.

Regarding claims 9 and 28, the insulator (Figure 6a, element 2; Figure 11, elements 21 and 22) is relatively thinner near the protrusion compared to the flat regions of the electron supply structure.

Regarding claims 10, 29 and 30, the insulator (Figure 6a, element 2; Figure 11, elements 21 and 22) has a substantially flat top surface local to the protrusion or can be considered to have an hourglass shape near the protrusion, as it is horizontally shaped as two larger areas joined by a thinner area.

Regarding claims 11 and 31, the insulator can be made of a diamond-like carbon, nitrides, carbides or oxynitrides of silicon, aluminum, titanium, tantalum, tungsten, hafnium, zirconium, vanadium, niobium, molybdenum, chromium, yttrium, scandium, nickel, cobalt, beryllium and magnesium (column 10, line 28 to column 11, line 22).

Regarding claims 12 and 32, the conductive substrate is formed of a metal on a glass substrate (column 18, line 54 to column 19, line 1).

Regarding claims 13 and 33, the metal coating on the conductive substrate can be made of aluminum or other metals (column 18, line 55).

Regarding claims 14 and 34, the metal coating of the conductive substrate is patterned (Figures 12B and 12C, element 1).

Regarding claims 15, 16, 35 and 36, the top conductive layer (Figure 11, element 33) is formed from a metal such as aluminum, tungsten, molybdenum, or gold (column 19, line 23).

Regarding claims 17 and 37, the top conductive layer (Figure 6a, element 3) is patterned.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 7 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iwasaki et al. (EP 1 117 118 A1) (of record) in view of Dalton et al. (3,717,790).

Iwasaki discloses an electron emitter device having an electron supply layer formed of a doped semiconductor, namely a silicon layer doped with boron or phosphorus.

Iwasaki lacks disclosure of how the doped silicon layer is formed or of the dopant distribution.

Dalton teaches the formation of a doped silicon layer, whereby the silicon is doped with boron and phosphorus ions via ion bombardment. Dalton teaches that ion bombardment is a well-known method of injecting dopants into a semiconductor, (column 2, lines 33-37). Dalton further teaches that the depth of ion bombardment is dependent on the energy of the ions being implanted, and that across the thickness of the silicon layer the density of the dopant will vary naturally (column 3, lines 37-40; column 4, lines 55-57).

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the doped semiconductor layer of Iwasaki to implant the ions in the semiconductor layer via ion bombardment, as Dalton teaches that as a commonly

used and reliable technique, and to have doping levels varying in the depth direction of the semiconductor layer, as Dalton teaches that such a result is the outcome of ion bombardment.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sharlene Leurig whose telephone number is (571) 272-2455. The examiner can normally be reached on Monday through Friday, 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nimesh Patel can be reached on (571) 272-2457. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sharlene Leurig

SL

ASHOK PATEL
PRIMARY EXAMINER